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PATENT SPECIFICATION

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DRAWINGS ATTACHED

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(54) IMPROVEMENTS IN OR RELATING TO PHASE EQUALISER CIRCUIT ARRANGEMENTS

(71) We THE MARCONI COMPANY LIMITED, a British company, of English Electric House, Strand, London, W.C.2, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to phase equaliser circuit arrangements and, though not limited exclusively to its application thereto, is primarily intended for phase equalisation in television transmitters.

The invention seeks to provide improved phase equaliser circuit arrangements suitable for use for compensating for variations in the time taken for the propagation of transmitted information, coincident with the so-called group delay, which is defined as the value of the ratio between the variation $d\phi$ of the phase angle ϕ and the corresponding variation $d\omega$ of the pulse ω at the operating frequency.

Variations in group delay as defined above occur whenever there is introduced into the transmitter and receiver circuits a filtering or equalising circuit the phase shift of which is non-linear with respect to frequency.

Examples of circuits introducing variable group delay and customarily to be found in T.V. transmitters are mixer circuits clipping the vestigial band corresponding with the sound carrier and low-pass filters for suppressing the radiation of the vision signal outside the working band. Examples of circuits introducing variable group delay and customarily included in T.V. receivers are clipping input and intermediate frequency filters and audio rejection circuits.

The effect of any circuit with phase-frequency non-linearity—e.g. any circuit such as the examples above given—is to modify the transients in the modulated wave carrying the required signal information, with resulting deformation of the information i.e. in the case of television transmission, distortion of the sound and/or vision signals.

It is common practice in television transmission to provide for compensating phase equalisation to prevent signal distortion as above described, by providing phase equaliser circuits of the inductance and capacity type and comprising a group of switchable quadripole phase equaliser circuits each having a different phase equalisation characteristic and to switch one or more of these sections into circuit in dependence upon the particular phase equalisation characteristic required. Arrangements of this nature have, however, the important defect that they are incapable of continuous adjustment to provide, at any particular time, the particular phase equalisation required, the said particular required phase equalisation being obtainable only by switching selection of the different sections provided. Moreover, in practice, such switchable arrangements involve the provision of a considerable number of sections of different characteristics. This is particularly the case with colour television transmission equipments where an unacceptably large number of switchable phase equaliser sections of different characteristics has to be provided if satisfactory results are to be achieved. In colour T.V. transmission equipment good phase equalisation is particularly necessary as respects the colour information since here any alteration of the transients due to group delay leads to colour alterations producing serious and often quite unacceptable distortion in colour reproduction at the receiver.

This invention therefore seeks to provide improved and simple phase equaliser circuit arrangements which will allow continuous correction of group delay within wide limits; which shall be adjustable in such manner as to enable a very close approximation to a linear phase-frequency characteristic to be obtained within the useful frequency; which shall not limit the frequency band of a T.V. transmitter or other equipment to which it is applied; and whose input and output impedances and insertion loss (i.e. signal attenuation) may be varied within adequately wide limit to allow for good impedance

[Price 25p]

matching with other circuits in a T.V. transmitter or receiver.

According to this invention an adjustable phase equaliser circuit arrangement suitable for use for compensating for non-linear phase/frequency characteristics in television transmitters and receivers includes at least one section comprising a T-network having a parallel adjustable inductance-capacity circuit in the series arm, a resistance in the shunt arm, an additional resistance in series in the series arm on the input side of said inductance capacity circuit and a further shunt resistance on the output side of said inductance-capacity circuit.

The invention is illustrated in and further explained in connection with the accompanying drawings in which:—

Figures 1 and 2 are diagrams of known quadripole section and are provided for purposes of preliminary explanation:

Figure 3 is a diagram of an embodiment of this invention:

Figure 4 is an equivalent circuit related to Figure 3:

Figure 5 shows a phase equaliser consisting of a number of sections each as illustrated in Figure 3, and interposed amplifiers.

The known phase equaliser quadripole section 1 shown in Figure 1 is of lattice configuration. In the unbalanced form it includes an LC circuit comprising an inductance 2 and a capacity 3 between the terminals A & C and, a single diagonal connection including the resistance 4 between the terminals A & D. In the balanced form it also includes the parts shown in broken lines.

The known section shown in Figure 2 is a T-section with the inductance 2 and capacity 3 in parallel between terminals A & C. The resistor 4 is connected between the direct connection 5 between terminals B & D and the mid-point of the inductance.

Theoretically the sections shown in Figures 1 and 2 require, for correct impedance matching, a voltage input source of zero impedance to be connected between the input terminals A & B and a load circuit of infinite impedance to be connected between the output terminals C & D. The frequency band pass is substantially flat and horizontal regardless of the values of R, L & C (R is the value of the resistance) provided (in the case of Figure 2) that there is unity coupling between the two sections 2_1—2_2 of the inductance on either side of its mid-point and provided that spurious inductances and capacitances are negligible. In the practical case, however, insertion loss, i.e. attenuation, exists; the input source is of low but not zero output impedance; and load is of high (but not infinite) impedance.

Figure 3 shows an improved phase equaliser section in accordance with this invention. As will be seen it is also a T-section but includes, in addition to the adjustable inductance 2 and adjustable capacity 3 and the resistance 4, the added resistances 6 and 7.

The insertion loss α can be deduced from a consideration of the equivalent resistive circuit shown in Figure 4 and is given by the equation:

$$\alpha = \frac{R_0 R_2}{R_1(R_0 + R_2) + R_0 + R_2},$$

where R_0, R_1 and R_2 represent respectively the values of resistors 4, 6 and 7 described above.

For an insertion loss of 6 dB the values of the resistors are, respectively, $R_1 = 120$ ohms, $R_2 = 150$ ohms and $R_3 = 750$ ohms. In Figure 3, G represents the input voltage source.

The insertion loss can be made good by gain provided by an amplifier in series with the section.

Preferred equaliser arrangements in accordance with the invention comprise a plurality of sections as shown in Figure 3 connected in cascade with interposed amplifiers for nullifying insertion losses. Such an arrangement is shown in Figure 5 in which 1a and 1b are sections each as shown in Figure 3 and 8a, 8b and 8c are the inserted amplifiers.

By varying the adjustable elements 2 and 3 in the sections a ratio of variation of 1 to 4 is readily obtainable.

Variation of the inductance 2 will alter the frequency spectrum of the group delay provided and variation of the capacity 3 will alter both the amplitude and the frequency spectrum of said delay.

By adjustment of the reactive elements 2 and 3 therefore it is possible to obtain practically any response curve, to suit the input signal present.

Resistive loss in the coil used in practice to provide the inductance 2 will affect the passband and, therefore, it is preferred, in carrying out the invention to provide for compensating for this by making the resistance 7 variable e.g. as shown for the section 1a of Figure 5 by constituting it by a fixed portion (referenced 7) in series with an adjustable portion (referenced 7a).

It is advantageous to constitute the inductance 2 by twin conductor windings, one for each of the portions on either side of the tap to which the resistance 4 is connected and to connect these sections in series. In this way a coupling factor that is substantially equal to unity is obtainable between the two portions.

In the arrangement shown in Figure 5, which is suitable for use for providing phase equalisation in a T.V. transmitter, the amplifiers provide a high input impedance and a low output impedance. They are D.C. coupled to avoid loss or attenuation of the vision signal at low frequencies.

In practice an arrangement consisting of three equaliser sections as described and illustrated and four amplifiers, one at the input end, one at the output end and one between each two successive sections can be adjusted to provide adequate correction of group delay for the great majority of known types of television transmitter.

WHAT WE CLAIM IS:—

1. An adjustable phase equaliser circuit arrangement suitable for use for compensating for non-linear phase/ frequency characteristics in television transmitters and receivers said arrangement including at least one section comprising a T-network having a parallel adjustable inductance-capacity circuit in the series arm, a resistance in the shunt arm, an additional resistance in series in the series arm on the input side of said inductance capacity circuit and a further shunt resistance in the output side of said inductance-capacity circuit.

2. An arrangement as claimed in claim 1 wherein the section comprises lumped constant elements comprising an adjustable inductor in parallel with an adjustable capacitor in the series arm, a separate additional series resistor and a separate further shunt resistor.

3. An arrangement as claimed in claim 2 wherein the inductor consists of twin windings connected in series each providing a portion of the inductance and with substantially unity coupling between them.

4. An arrangement as claimed in any of the preceding claims wherein said further resistor is adjustable.

5. An arrangement as claimed in any of the preceding claims 1 to 4 and comprising a plurality of sections in cascade and each successive two of which are separated by a D.C. coupled amplifier of high input impedance and low output impedance.

6. An arrangement as claimed in claim 5 wherein the first of the cascaded sections is preceded by a D.C. coupled amplifier of high input impedance and low output impedance and the last of said cascaded sections is followed by a D.C. coupled amplifier of high input impedance and low output impedance.

7. Adjustable phase equaliser circuit arrangements substantially as herein described with reference to Figure 3 or Figure 5 of the accompanying drawings.

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1 SHEET

COMPLETE SPECIFICATION

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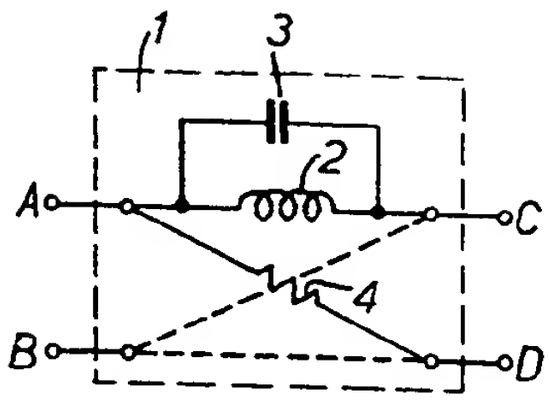

FIG. 1.

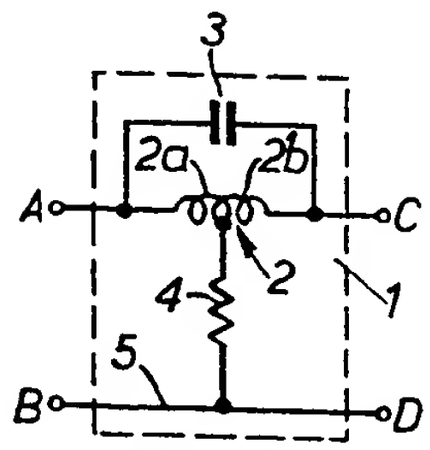

FIG. 2.

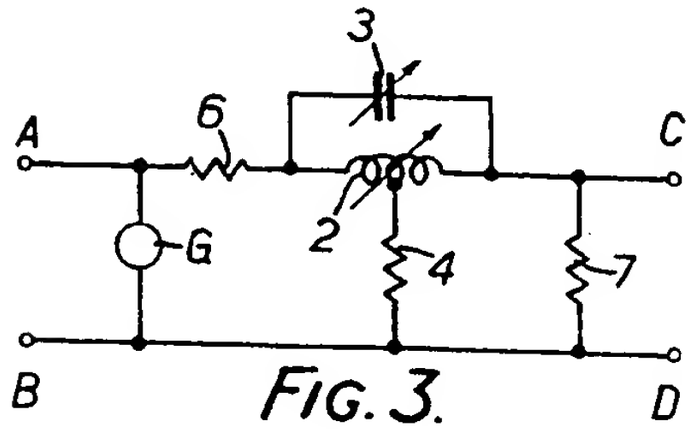

FIG. 3.

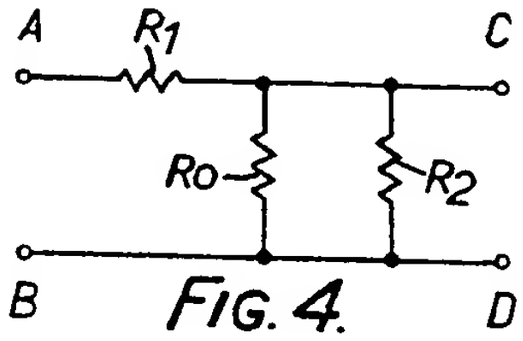

FIG. 4.

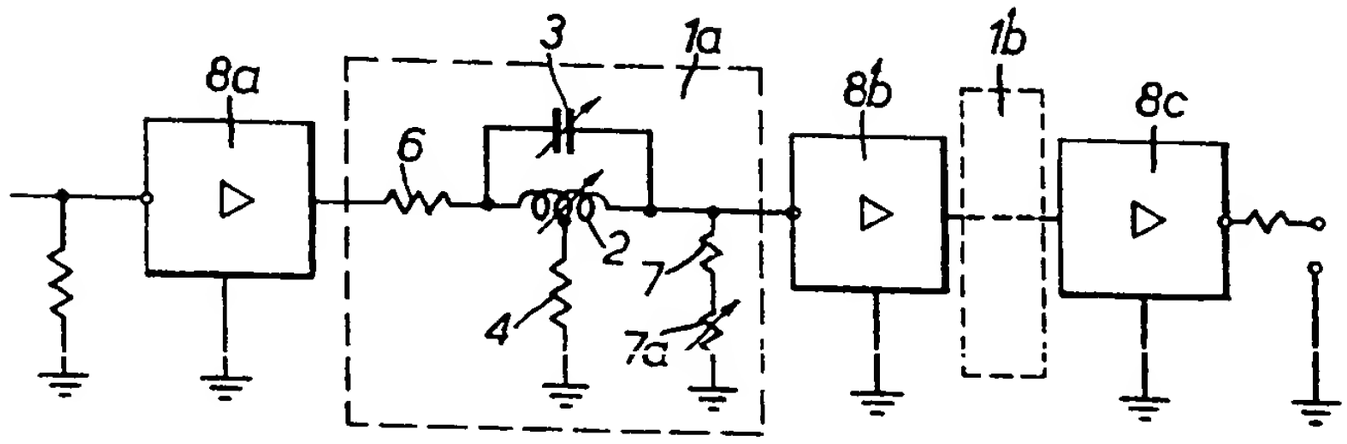

FIG. 5.